Abstract of the Disclosure

An integrated circuit driver includes an output stage having source drain paths of a PFET and NFET connected in series with each other across DC power supply terminals. A pair of CMOS inverters simultaneously responsive to a bilevel signal drive gate electrodes of the PFET and NFET. The inverters include resistors connected to NFET and PFET devices which function as voltage controlled switched capacitors respectively connected in shunt with gate electrodes of the output stage PFET and NFET. The inverters, resistors and capacitors prevent the output stage PFET and NFET from being on simultaneously.